A4

LSI design. Ultimately, the LSI design foundry prepares the netlist using this scan FF d2403. Thereafter, the netlist d2403 is passed to the client of LSI design.

**IN THE CLAIMS:**

**Please cancel Claims 2-16 without prejudice or disclaimer.**

A5

**1. (Amended) A storage circuit comprising:**

**a first logic gate for receiving a first signal and a second signal, and for selectively outputting either the first signal or the second signal in accordance with a control signal;**

**a first storage element for receiving a clock signal, for storing an output signal of the first logic gate in response to the clock signal, and for outputting the stored signal as a third signal in response to the clock signal; and**

**a second logic gate for receiving the third signal from the first storage element, said second logic gate fixing an output signal thereof, regardless of the received third signal, in response to the control signal;**

wherein the storage circuit, having a first output and a second output, outputs the third signal through the first output, and the output signal of the second logic gate through the second output.

Please add the following claims:

17. (New) A storage circuit having first and second outputs, comprising:

a first logic gate for receiving a first signal and a second signal, and for selectively outputting either the first signal or the second signal in accordance with a control signal;

a first storage element, having a master latch and a slave latch, wherein the master latch inputs an output signal of the first logic gate and latches the output signal of the first logic gate in response to the clock signal, and the slave latch inputs an output signal of the master latch and passes the output signal of the master latch to the first output of the storage circuit in response to an inverted clock signal;

a second logic gate for receiving the output signal of the master latch, and for outputting the output signal of

the master latch to the second output of the storage circuit in response to the control signal.

18. (New) A storage circuit comprising:

a first logic gate for receiving a first signal and a second signal, and for selectively outputting either the first signal or the second signal in accordance with a first control signal;

a first storage element for receiving a clock signal, for storing an output signal of the first logic gate in response to the clock signal, and for outputting the stored signal as a third signal in response to the clock signal; and

a second logic gate for receiving the third signal from the first storage element, said second logic gate fixing an output signal thereof, regardless of the received third signal, in response to a second control signal,

wherein the storage circuit, having a first output and a second output, outputs the third signal through the first output, and the output signal of the second logic gate through the second output.

19. (New) A storage circuit according to claim 18,

wherein the second control signal is fixed to a low level earlier than the first control signal at a time of a transition from a scan-in operation to a logic test operation.

20. (New) A semiconductor integrated circuit comprising:

a first storage circuit including first and second input terminals, first and second output terminals, a first control terminal for receiving a control signal, first and second logic gates, and a first storage element;

a logic circuit for receiving an output signal of the first output terminal of the first storage circuit, for performing a predetermined processing on the output signal, and for outputting a result of the processing; and

a second storage circuit including third and fourth input terminals, and a second control terminal for receiving the control signal,

wherein the first logic gate receives a first signal of the first input terminal and a second signal of the second input terminal, and selectively outputs either the first signal or the second signal in accordance with the control signal of the first control terminal;

wherein the first storage element receives a clock signal, stores an output signal of the first logic gate in response to the clock signal, and outputs the stored signal by way of a third signal in response to the clock signal;

wherein the second logic gate receives the third signal from the first storage element, the second logic gate fixing an output signal thereof, regardless of the received third signal, in response to the control signal of the first control terminal;

wherein the first storage circuit outputs the third signal through the first output terminal to the logic circuit, and the output signal of the second logic gate through the second output terminal to the second storage circuit; and

wherein the second storage circuit receives the output signal from the first storage circuit through the third input terminal and the output signal of the logic circuit through the fourth input terminal, and selectively stores either the output signal of the logic circuit or the first storage circuit in accordance with the control signal of the second control terminal.